Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **2A**
3. **OUT A**
4. **OUT B**
5. **1B**
6. **2B**
7. **VSS**
8. **1C**
9. **2C**
10. **OUT C**
11. **OUT D**
12. **1D**
13. **2D**
14. **VDD**

**.041”**

**12 11 10 9**

**13**

**14**

**1**

**8**

**7**

**6**

**2 3 4 5**

**MASK**

**REF**

**204011**

****

**.047”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .04”**

**Backside Potential: VDD or FLOAT**

**Mask Ref: 4011**

**APPROVED BY: DK DIE SIZE .041” X .047” DATE: 8/17/21**

**MFG: SILICON SUPPLY THICKNESS .014” P/N: CD4011B**

**DG 10.1.2**

#### Rev B, 7/19/02